Book Static Timing Analysis For Nanometer Designs A

This book serves as a hands-on guide to timing constraints in integrated circuit design. Readers will learn to maximize performance of their IC designs, by specifying timing requirements correctly. Coverage includes key aspects of the design flow impacted by timing constraints, including synthesis, static timing analysis and placement and routing. Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow, all within the context of Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints.

What other areas of the organization might benefit from the Static timing analysis team's improvements, knowledge, and learning? What may be the consequences for the performance of an organization if all stakeholders are not consulted regarding Static timing analysis? Who will provide the final approval of Static timing analysis deliverables? When a Static timing analysis manager recognizes a problem, what options are available? What role does communication play in the success or failure of a Static timing analysis project? Defining, designing, creating, and implementing a process to solve a challenge or meet an objective is the most valuable role... In EVERY group, company, organization and department. Unless you are talking a one-time, single-use project, there should be a process. Whether that process is managed and implemented by humans, AI, or a combination of the two, it needs to be designed by someone with a complex enough perspective to ask the right questions. Someone capable of asking the right questions and step back and say, 'What are we really trying to accomplish here? And is there a different way to look at it?' This Self-Assessment empowers people to do just that - whether their title is entrepreneur, manager, consultant, (Vice-)President, CxO etc... - they are the people who rule the future. They are the person who asks the right questions to make Static timing analysis investments work better. This Static timing analysis All-Inclusive Self-Assessment enables You to be that person. All the tools you need to an in-depth Static timing analysis Self-Assessment. Featuring 682 new and updated case-based questions, organized into seven core areas of process design, this Self-Assessment will help you identify areas in which Static timing analysis improvements can be made. In using the questions you will be better able to: - diagnose Static timing analysis projects, initiatives, organizations, businesses and processes using accepted diagnostic standards and practices - implement evidence-based best practice strategies aligned with overall goals - integrate recent advances in Static timing analysis and process design strategies into practice according to best practice guidelines Using a Self-Assessment tool known as the Static timing analysis Scorecard, you will develop a clear picture of which Static timing analysis areas need attention. Your purchase includes access details to the Static timing analysis self-assessment dashboard download which gives you your dynamically prioritized projects-ready tool and shows your organization exactly what to do next. Your exclusive instant access details can be found in your book.

As semiconductor technology is scaled and voltage level is reduced, the impact of the variation in power supply has become very significant in predicting the realistic worst-case delays in integrated circuits. The analysis of power supply noise is inevitable because high correlations exist between supply voltage and delay. Supply noise analysis has often used a vector-based timing analysis approach. Finding a set of test vectors in vector-based approaches, however, is very expensive, particularly during the design phase, and becomes intractable for larger circuits in DSM technology. In this work, two novel vectorless approaches are described such that increases in circuit delay, because of power supply noise, can be efficiently, quickly estimated. Experimental results on ISCAS89 circuits reveal the accuracy and efficiency of my approaches: in s38417 benchmark circuits, errors on circuit delay distributions are less than 2%, and both of my approaches are 67 times faster than the traditional vector-based approach. Also, the results show the importance of considering care-bits, which sensitize the longest paths during the power supply noise analysis.

Power is a valuable resource in embedded systems as the lifetime of many such systems is constrained by their battery capacity. Recent advances in processor design have added support for dynamic frequency/voltage scaling (DVS) for saving power. Recent work on real-time scheduling focuses on saving power in static as well as dynamic scheduling environments by exploiting idle and slack due to early task completion for DVS of subsequent tasks. These scheduling algorithms rely on a priori knowledge of worst-case execution times (WCET) for each task. They assume that DVS has no effect on the worst-case execution cycles (WCEC) of a task and scale the WCET according to the processor frequency. However, for systems with memory hierarchies, the WCEC typically does change under DVS due to frequency modulation. Hence, current assumptions used by DVS schemes result in a highly exaggerated WCET. The research presented contributes novel techniques for tight and flexible static timing analysis particularly well-suited for dynamic scheduling schemes. The technical contributions are as follows: (1) The problem of changing execution cycles due to scaling techniques is assessed. (2) A parametric approach towards bounding the WCET statically with respect to the frequency is proposed. Using a parametric model, the effect of changes in frequency on the WCEC can be captured and, thus, the WCET over any frequency range can be accurately modeled. (3) The design and implementation of the frequency-aware static timing analysis (FAST) tool, based on prior experience with static timing analysis, is discussed. (4) Experiments demonstrate that the FAST tool provides safe upper bounds on the WCET, which are tight. The FAST tool allows the capture of the WCET of six benchmarks using equations that overestimate the WCET by less than 1%. FAST equations can also be used to improve existing DVS scheduling schemes to ensure that the effect of frequency scaling on WCET is considered and that the WCET use.

iming, timing, timing! That is the main concern of a digital designer charged with designing a semiconductor chip. What is it, how is it T described, and how does one verify it? The design team of a large digital design may spend months architecting and iterating the design to achieve the required timing target. Besides functional verification, the t- ing closure is the major milestone

which dictates when a chip can be - leased to the semiconductor foundry for fabrication. This book addresses the timing verification using static timing analysis for nanometer designs. The book has originated from many years of our working in the area of timing verification for complex nanometer designs. We have come across many design engineers trying to learn the background and various aspects of static timing analysis. Unfortunately, there is no book currently ava- able that can be used by a working engineer to get acquainted with the - tails of static timing analysis. The chip designers lack a central reference for information on timing, that covers the basics to the advanced timing veri- cation procedures and techniques.

Synopsys' PrimeTime is widely used for static timing analysis and timing signoff solutions nowadays. However, PrimeTime has its two limitation. Firstly, it is unable to work on some customized fabric where the circuit consist not only the standard cells and wires as in conventional circuit. Secondly, PrimeTime reports the timing of the design not as accurate in deep nanotechnology. The error could sometimes be as large as 15% compare to the real case. In this article, we proposed a novel STA approach that combines the HSpice simulation and PrimeTime analysis to provide timing accuracy that is comparable to HSpice. This approach is very flexible that could work on any non-standard customized circuit including SRAM cell or customized circuit that containing pass transistors. The thesis also introduced a customized design circuit named Field Programmable Transistor Array (FPTA) as test case to practically proved the feasibility of the new STA approach. The simulation result shows that the proposed approach could work on nonstandard circuit and provide the accuracy that is extremely close to Spice simulation.

Please note that the content of this book primarily consists of articles available from Wikipedia or other free sources online. Pages: 32. Chapters: Contamination delay, Delay calculation, Duty cycle, Dynamic timing verification, Propagation delay, Race condition, Retiming, Static timing analysis, Statistical static timing analysis, Timing closure.

This dissertation reports on a new methodology to characterize and simulate a standard cell library to be used for statistical static timing analysis. A compact variation-aware timing model for a standard cell in a cell library has been developed. The model incorporates variations in the input waveform and loading, process parameters, and the environment into the cell timing model. Principal component analysis (PCA) has been used to form a compact model of a set of waveforms impacted by these sources of variation. Cell characterization involves determining equations describing how waveforms are transformed by a cell as a function of the input waveforms, process parameters, and the environment. Different versions of factorial designs and Latin hypercube sampling have been explored to model cells, and their complexity and accuracy have been compared. The models have been evaluated by calculating the delay of paths. The results demonstrate improved accuracy in comparison with table-based static timing analysis at comparable computational cost. Our methodology has been expanded to adapt to interconnect dominant circuits by including a resistive-capacitive load model. The results show the feasibility of using the new load model in our methodology. We have explored comprehensive accuracy improvement methods to tune the methodology for the best possible results. : The following is a summary of the main contributions of this work to the statistical static timing analysis.

Statistical timing analysis is an area of growing importance in nanometer te- nologies, as the uncertainties associated with process and environmental var- tions increase, and this chapter has captured some of the major efforts in this area. This remains a very active field of research, and there is likely to be a great deal of new research to be found in conferences and journals after this book is published. In addition to the statistical analysis of combinational circuits, a good deal of work has been carried out in analyzing the effect of variations on clock skew. Although we will not treat this subject in this book, the reader is referred to [LNPS00, HN01, JH01, ABZ03a] for details. 7 TIMING ANALYSIS FOR SEQUENTIAL CIRCUITS 7.1 INTRODUCTION A general sequential circuit is a network of computational nodes (gates) and memory elements (registers). The computational nodes may be conceptualized as being clustered together in an acyclic network of gates that forms a c- binational logic circuit. A cyclic path in the direction of signal propagation 1 is permitted in the sequential circuit only if it contains at least one register . In general, it is possible to represent any sequential circuit in terms of the schematic shown in Figure 7.1, which has I inputs, O outputs and M registers. The registers outputs feed into the combinational logic which, in turn, feeds the register inputs. Thus, the combinational logic has I + M inputs and O + M outputs.

A novel waveform model for improving the accuracy of gate delay prediction in static timing analysis has been developed. Moreover, a full methodology on modeling complex circuits such as unbuffered latches for timing analysis has been developed. Since variations in process, environment, and temperature have become very important, a simple path-based statistical static timing analysis algorithm has also been proposed. The algorithm models timing variations accurately for latest high-performance microprocessors.

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"Static timing analysis is a key process to guarantee timing closure for modern IC designs. However, additional pessimism can significantly increase the difficulty to achieve timing closure. Common path pessimism removal (CPPR) is a prevalent step to achieve accurate timing signoff. To speed up the existing exhaustive exploration on all paths in a design, this thesis introduces a fast multi-threading timing analysis for removing common path pessimism based on block-based static timing analysis. Experimental results show that the proposed method has faster runtime in removing excess pessimism from clock paths."--Abstract, page iii.

Manufacturing process variations lead to circuit timing variability and a corresponding timing yield loss. Traditional corner analysis consists of checking all process corners (combinations of process parameter extremes) to make sure that circuit timing constraints are met at all corners, typically by running static timing analysis (STA) at every corner. This approach is becoming too expensive due to the increase in the number of corners with modern processes. As an alternative, we propose a linear-time approach for STA which covers all process corners in a single pass. Our technique assumes a linear dependence of delays and slews on process parameters and provides tight bounds on the worst-case circuit delay and slew. It exhibits high accuracy (up to 2%) in practice and, if the circuit has m gates and n relevant process parameters, the complexity of the algorithm is Omn .

The Art of Timing Closure is written using a hands-on approach to describe advanced concepts and techniques using Multi-Mode Multi-Corner (MMMC) for an advanced ASIC design implementation. It focuses on the physical design, Static Timing Analysis (STA), formal and physical verification. The scripts in this book are based on Cadence®

Encounter SystemTM. However, if the reader uses a different EDA tool, that tool’s commands are similar to those shown in this book. The topics covered are as follows: Data Structures Multi-Mode Multi-Corner Analysis Design Constraints Floorplan and Timing Placement and Timing Clock Tree Synthesis Final Route and Timing Design Signoff Rather than go into great technical depth, the author emphasizes short, clear descriptions which are implemented by references to authoritative manuscripts. It is the goal of this book to capture the essence of physical design and timing analysis at each stage of the physical design, and to show the reader that physical design and timing analysis engineering should be viewed as a single area of expertise. This book is intended for anyone who is involved in ASIC design implementation -- starting from physical design to final design signoff. Target audiences for this book are practicing ASIC design implementation engineers and students undertaking advanced courses in ASIC design.

Keywords: real-time scheduling, frequency scaling, real-time systems, dynamic voltage scaling.

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The primary aim of this book is to introduce the concepts of FPGA timing based on Synopsys style timing analysis in a simplified yet concise way with emphasis on clear understanding of concepts and practical aspects away from syntax clutter or excessive sdc based examples.

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